Examination SS 2013

Communication Systems and Protocols

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Communication Systems and Protocols
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Prerequisites for the examination

Aids

- Allowed aids for the examination are writing utensils, a ruler, a non-programmable calculator and a single sheet of A4 paper with self- and hand-written notes. Writing may be on a single side of the paper only. The use of own concept paper is not allowed.
- Use only indelible ink - use of pencils and red ink is prohibited.
- Other aids than that mentioned above is strictly forbidden. This includes any type of communication to other people.

Duration of the examination

120 minutes

Examination documents

The examination comprises 30 pages (including title page). Answers may be given in English or German. A mix of language within a single (sub)-task is not allowed. In your solution mark clearly which part of the task you are solving. Do not write on the backside of the solution sheets. If additional paper is needed ask the examination supervisor. It may not be possible to finish all tasks within the duration of the examination. This will be accounted for within the grading of the exam.

You will not be allowed to hand in your examination and leave the lecture hall in the last 30 minutes of the examination.

At the end of the examination: Stay at your seat and put all sheets into the envelope. Only sheets in the envelope will be corrected. We will collect the examination.

Task 1 Error Protection

Task 1.1 Error Detection

A) Name two methods for error detection within a communication protocol based on redundancy.

B) To which extend can Parity Checking be used to detect burst errors? Justify your answer.

Task 1.2 CRC-Calculation

The bitstream 10110011 shall be coded and transmitted using the generator polynomial $g(x)=x^6+x^5+x^3+x^2+1$.

A) Give the bitstring for the given generator polynomial

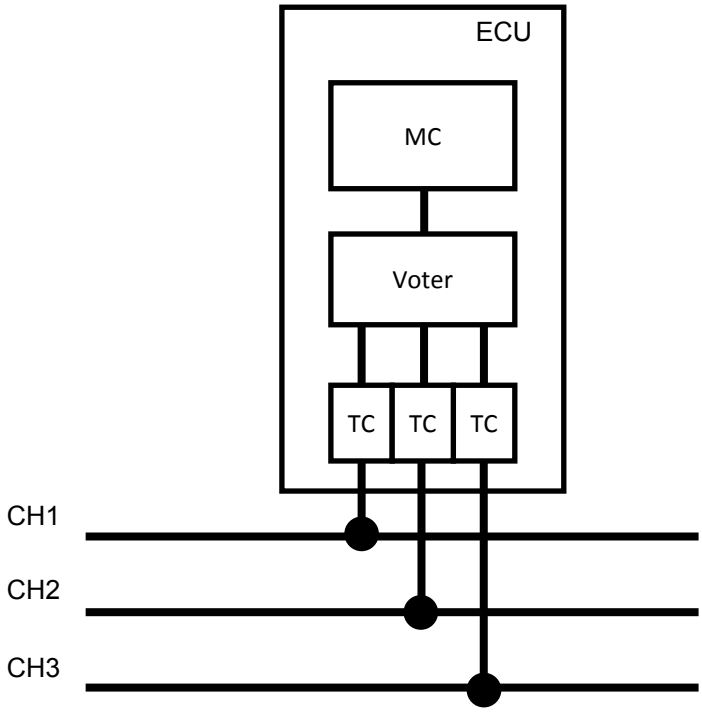
B) Determine the bitstream as it is being transmitted.

C) With a transmission system that uses CRC for error protection, a sender transmits the following bitstream: 10110011000011.
Carry out the CRC error detection scheme of the receiver, assuming that the generator polynomial $g(x)= x^6+x^5+x^3+x^2+1$ has been used. What does the receiver conclude from the result?

D) Given is the bitstring 1011 of a generator polynomial. Draw the full (not the simplified) hardware realization of the decoder by means of flip flops, XOR and AND gates.

Task 1.3 External Redundancy

The figure below illustrates a setup of a bus system using multiple parallel channels (CH1, CH2, CH3). Data that is received by an electronic control unit (ECU) is read off the bus via transceivers (TC). Subsequently it passes a voter before it is processed within a microcontroller (MC).



A) What is the task of the voter?

B) Assume the following:
1) Only a single error is possible at any point in time in the whole system
2) Errors are only injected over bus lines
3) Only external redundancy is used for error detection.
Question: What is the minimal number of redundant channels necessary in order to be able to detect transmission errors? Justify your answer.

C) Assume the same preconditions as in B). How many redundant channels are necessary in order to be able to correct transmission errors? Justify your answer.

Task 2 Media Access

Task 2.1 Multiple use of media

A) For transmitting data of multiple nodes at the same time different access schemes exist. Name two access schemes other than CDMA.

B) Give the Walsh-functions for the transmission of four nodes at the same time.

Function 1				
Function 2				
Function 3				
Function 4				

Table 2.1: Walsh-functions

For a CDMA access scheme the first three chips of the Walsh-functions from the subtask above got lost. Sending the bits listed in table 2.2 the signal **0 4 0 0** can be measured on the medium.

	Walsh-function				**send bit**
A				**-1**	**1**
B				**+1**	**0**
C				**-1**	**0**
D				**+1**	**1**

Table 2.2: CDMA scheme using Walsh-functions

C) Complete table 2.2 with the correct missing chips. Justify your answer by giving all your calculation steps or your complete reasoning.

D) What are the general advantages and disadvantages of CDMA? (list one advantage and one disadvantage)

Task 2.2 Arbitration

A) For the arbitration of four nodes a Tap-line model is used. Draw a Tap-line model with four nodes. Label all used signals. Give a short explanation (one sentence) of each of the different types of signals used in this scheme. Mark the arbiter in your scheme and briefly explain its basic function (ca. 3 sentences).

A system using centralized daisy-chaining is shown in figure 2.1. An exemplary arbitration cycle of the system is shown in figure 2.2.

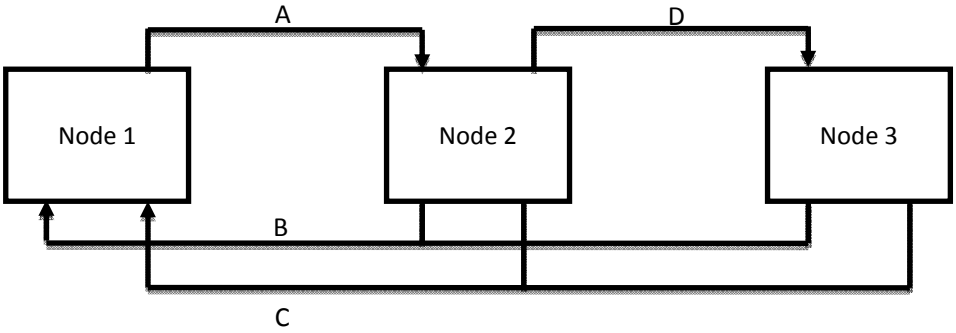


Figure 2.1: Centralized Daisy-chain

B) Assign the correct signals of figure 2.1 to the signals shown in the diagram below (figure 2.2). Justify your choice of assignment with a few sentences.
What node is sending data at which point in time? Complete the diagram (figure 2.2) accordingly.

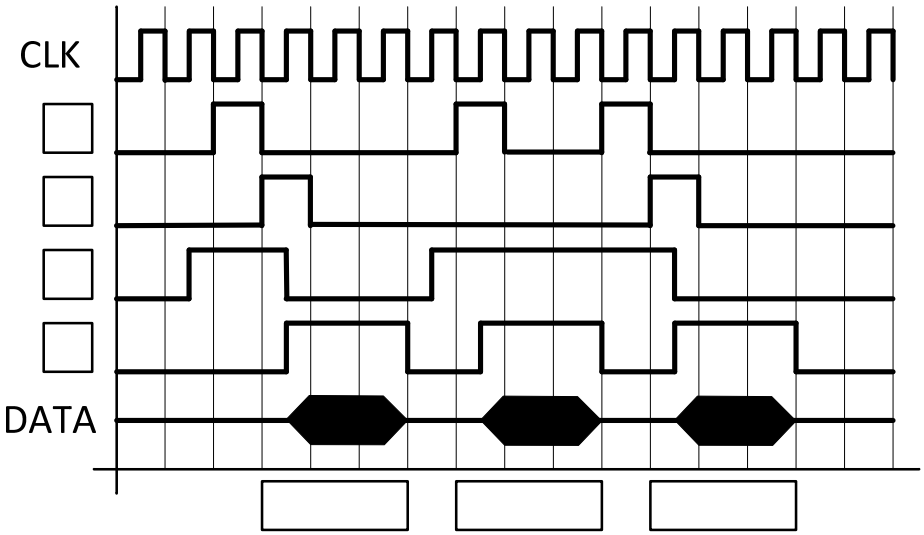


Figure 2.2: Signal flow for Daisy-chain

In the decentralized Daisy-chain shown in figure 2.3 a scheduling should be done. The different nodes will set a request at the times given in table 2.3. Only after successful transmission the nodes will remove their request. The sending of the data always needs exactly one time step. This includes token passing and the time needed for the arbitration.

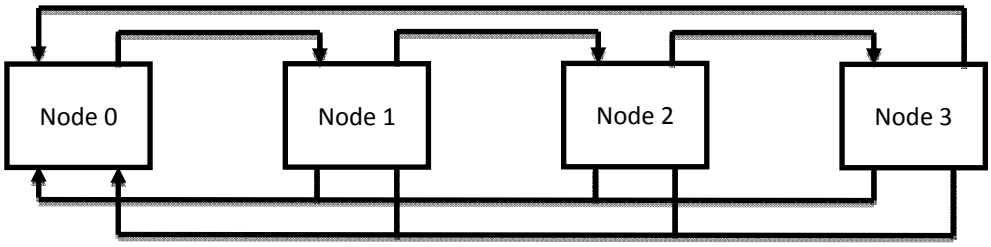


Figure 2.3: Decentralized Daisy-chain

time	Nodes that assert a sending request signal
t_1	Node 2 and Node 3
t_2	Node 1
t_3	Node 0
t_4	Node 0 and Node 1

Table 2.3: Time of sending nodes

C) Complete Table 2.4 according to the specified arbitration scheme.

time	Sending node
t_0	Node 0
t_1	
t_2	
t_3	
t_4	
t_5	
t_6	

Table 2.4: Solution of Daisy-chain scheduling

Task 3 Synchronization

Task 3.1 Synchronization methods

A) Characterize the synchronization methods in the table below with respect to the given transmission types.

Transmission methods	Parallel	Serial	Synchronous	Asynchronous
Shared/dedicated clock line				
Start-stop mode				
Suitable line code				
Handshake mode				
Scrambler				

B) Using the table below, compare the given methods with respect to the synchronization characteristics/properties and cost. Only one example per cell is necessary.

Method	Advantages	Disadvantage
Dedicated clock line		
Suitable line code		
Scrambler		

Task 3.2 Hand-shaking partners

A communication system is given in Figure 3.1. The sender's clock frequency is 1 MHz, the receiver's is 200 kHz. Both partners work synchronously to their own clock signal and try their best to communicate as fast as possible. They apply a half-duplex hand-shake protocol corresponding to Figure 3.1 for the high-level synchronization.

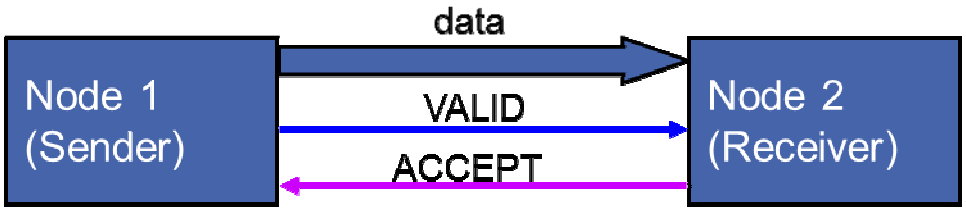


Figure 3.1: Communication system applying half-duplex hand-shake procedure

A) In Figure 3.2, the sensitive clock edges of the sender and the receiver as well as the signals' values for the first sender's clock period are shown. In order to avoid violations of setup and hold times, the data is put onto the bus and one clock cycle later the *valid* signal is set to '1' by the sender. The receiver will also set the *accept* signal one clock cycle after having received the data. Fill in the progression of all signal lines until the end of the time scale.

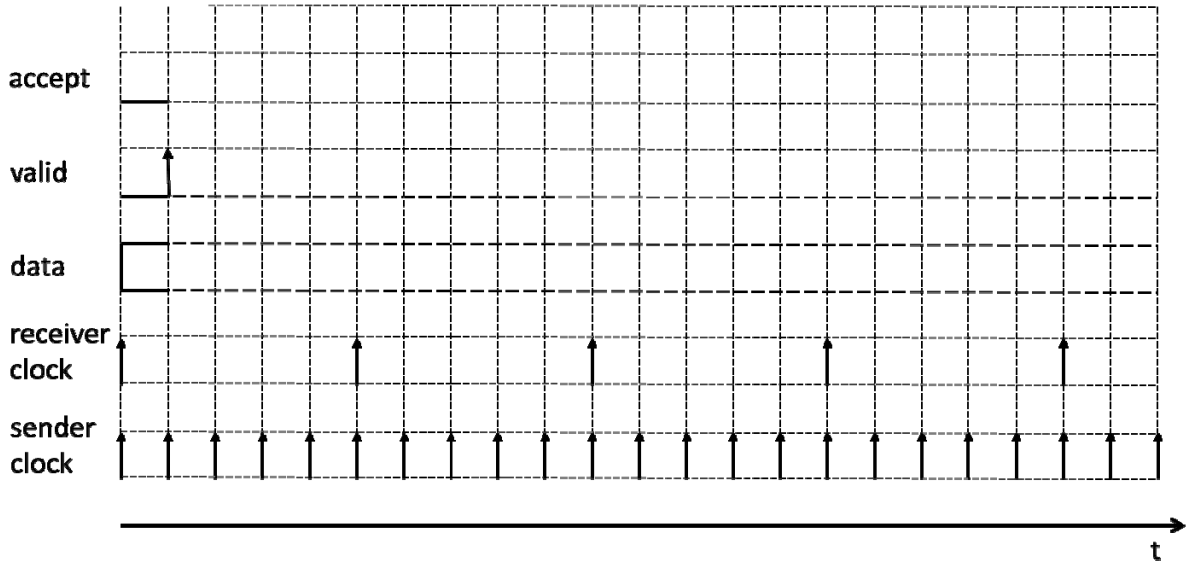


Figure 3.2: Signal progression diagram

B) Is this kind of synchronization free from error in this specific case? Justify your answer.

C) Propose a better solution for this communication scenario.

Task 3.3 Against noise with tied hands

You are to design a data communication system with a data rate of 25 Mbps. However, the given communication channel is noisy. Statistics shows that during one bit interval, one noise pulse, which causes the signal to be misinterpreted (bit flipping), may occur with a maximum duration of 15 ns. Due to resource constraints, neither are you allowed to switch to another channel, nor is it possible to modify the sender, which does not integrate any mechanism for error correction. What can you do in order to make your system works correctly (statistically seen)? Rationalize your solution.

Task 4 Data Transmission

Task 4.1 Transmission Rate

The CSMA/CD media access control as used in Ethernet includes a collision detection method. Thereby, a sender transmits a jam signal if it detects another signal while transmitting a frame. The jam signal must propagate to all receivers before the transmission ends. This introduces a minimum frame size for Ethernet that is coupled to the maximum wire length. The minimum frame transmission time must be higher than the time required passing a maximum length wire twice.

A) Calculate the minimum frame size in bytes of an Ethernet network running at 100 Mbit/s over a coaxial cable with the following parameters?

Transmission rate: 100 Mbit/s

Maximum cable length: 500 m

Propagation speed of coaxial cable: 200000 km/s

B) Calculate the minimum efficiency of the transmission system when sending only dataframes with minimum frame size and an overhead of 100 bits per frame are required.

C) The maximum frame size for ethernet is 1500 bytes. Would you use CSMA/CD together with 10 Gbit Ethernet? Please explain your answer.

Task 4.2 Shannon Limit

A) What is the Shannon Limit?

B) Calculate the Shannon Limit for a channel with 1000 Hz bandwidth and a S/N of 127. Give the result in bits/second.

C) Calculate the required signal-to-noise ratio (SNR) in dB for a channel with 1 MHz bandwidth and a transfer rate of 3 Mbit/s.

Task 5 Physics

Task 5.1 General questions

A) What are parameters of a periodic signal? Name 2 parameters.

B) Several modulation techniques were discussed in the lecture. Name 3 of them and describe shortly their functionality.

C) What does cut off frequency mean?

Task 5.2 DA/AD-Conversion

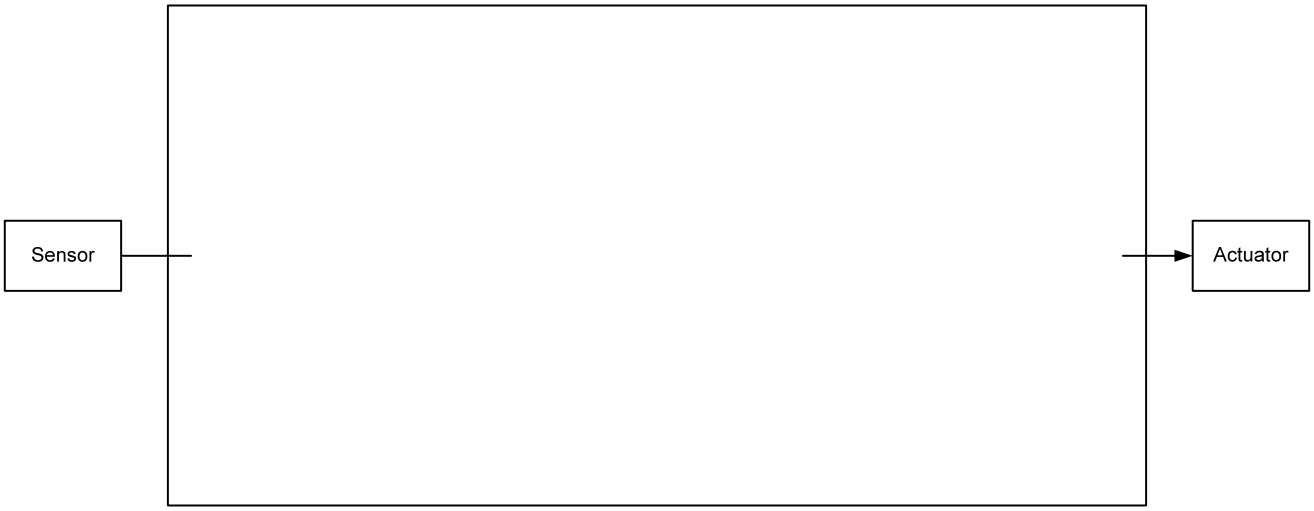
A) What is the minimum frequency an analog signal has to be sampled with in order to allow perfect reconstruction of the analog signal? Give the equation and the name of the theorem.

B) Why and when is a sample & hold element necessary?

C) Oversampling: Explain what oversampling means and name the advantages.

Task 5.3 Modulation

An analog signal is send from a sensor to an analog actuator. It has to be modulated with frequency shift keying. Draw in a block diagram the complete transmission chain of the signal and name all necessary blocks with their corresponding signals. Give a short description of the task of each block and signal.



Task 5.4 Reflection on wires

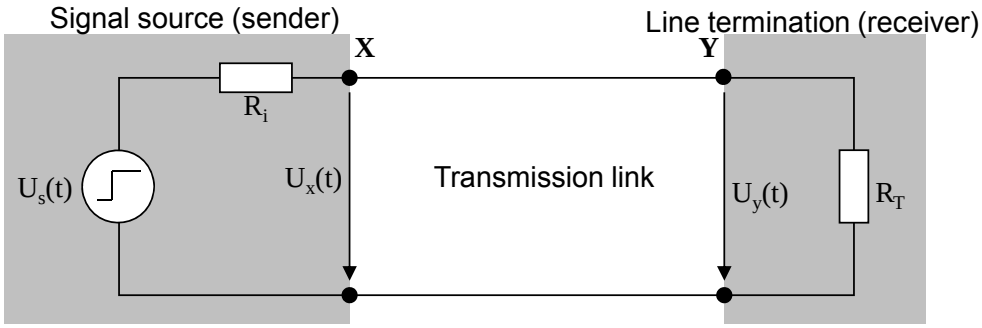


Figure 5.1: Test Setup

A) In Figure 5.1 an assembly is considered, consisting of a voltage source with an internal resistance $R_i = 75\Omega$ as sender and a receiver with $R_T = 250\Omega$. The DC resistance of the line is zero. Calculate the value of the wave resistance at the time of t=0.

At the time t=0 the voltage U_s of the sender changes from 0V to 6V and is constant afterwards. The runtime of a wave on the wire is t_d. The voltage u_x at the time of t=0 is $U_x(0) = 4V$.

B) Calculate the reflection factor on receiver side of the test setup in Figure 5.1.

C) Which value has the reflection factor on receiver side if the termination resistance is ∞?

D) When does a perfect wire adaption exist?

Task 6 Practical Aspects of Communication Systems

Task 6.1 General Questions

A) Which factors are constraining the throughput of parallel busses? Name 2 factors.

B) What is the difference between synchronous and asynchronous communication?

C) How many layers does the TCP/IP internet reference model have?

D) Explain the difference between a LAN switch and a router.

Task 6.2 Serial Protocol

In Figure 6 a serial protocol is given.

PREAMBLE	START	ADDR	EXP	CMD	BCNT	STATUS	DATA	CHK

Preamble: 5 bytes 0xFF (settling time)

Start character: 1 byte

Address: source and destination, 1 byte

Expansion field: 1 byte

Command: 1 byte

Byte count: 1 byte (≥0x02)

Status: 2 byte

Data: (BCNT-2) bytes

Checksum: 1 byte

Figure 6.1: Serial protocol with 9 fields

A) Is the total length of a message fixed or variable? Please justify your answer and specify the total length if it is fixed or the minimum and maximum length of the packet if it is of variant size

B) Which field(s) is/are indicating that the protocol from Figure 6.1 is used for an asynchronous communication? How could a resynchronization work here?

Task 6.3 Development of a custom bus

For a specialized system-on-chip a synchronous on-chip bus for communication between a master module and several slave modules needs to be developed.

The requirements are:

- Clock synchronous
- Parallel bus
- No tri-state drivers
- Separate bus lines for read data and write data
- Width of data busses is 32 bit
- Address range from 0x0000 to 0xFFFF in each slave
- Maximum 16 slave modules possible

A) Please draw a “black box” of the master module, containing all necessary ports. In case of bus lines, please mark the bus widths.

B) Is there a difference in the slave modules concerning the signals or the widths? Justify your answer?

Task 6.4 Timing diagram of asynchronous bus

In Figure 7 an asynchronous parallel bus for interfacing e.g. NOR Flash memories is given. A description of the interface signals is given in Table 6.1.

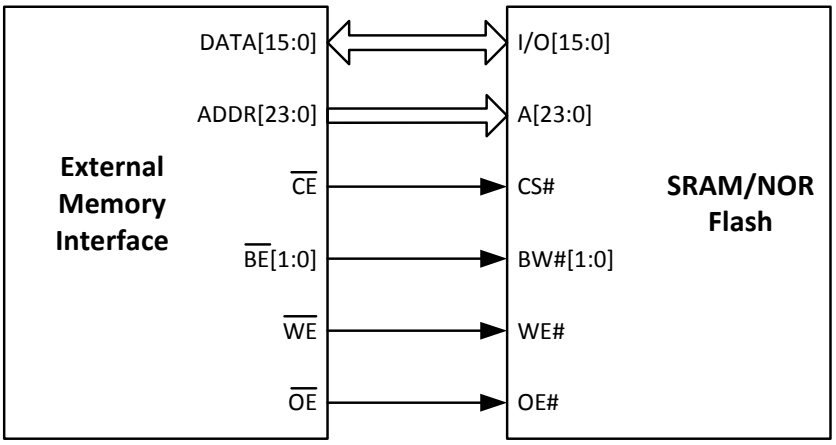


Figure 6.2: External memory interface with asynchronous bus, connected to a Flash memory

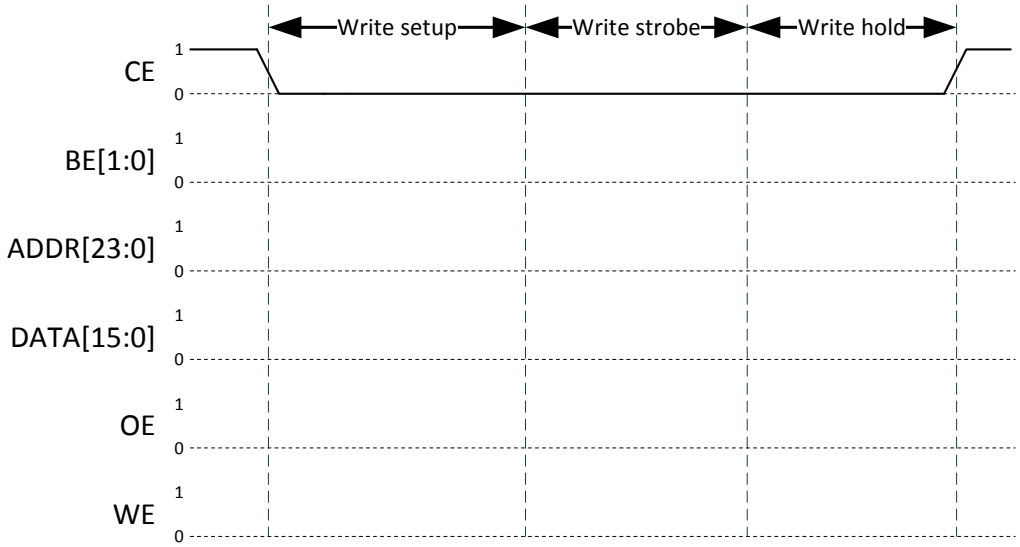
Port	Description
DATA [15:0]	Data I/O pins. 16/8-bit bidirectional data path for I/O.
ADDR [23:0]	External address outputs.
CE[3:0]	Chip select for CE space. Active-low chip select for memory spaces 0 to 3.
BE[1:0]	Active-low byte enables (Upper and lower). Individual bytes or half-words can be selected: “00” = data on DATA[15:0], “01” = data on DATA[15:8], “10” = data on DATA[7:0]
OE	Active-low output enable. Low during read access period.
WE	Active-low write enable. Low during write transfer strobe period.

Table 6.1: Description of the interface signals

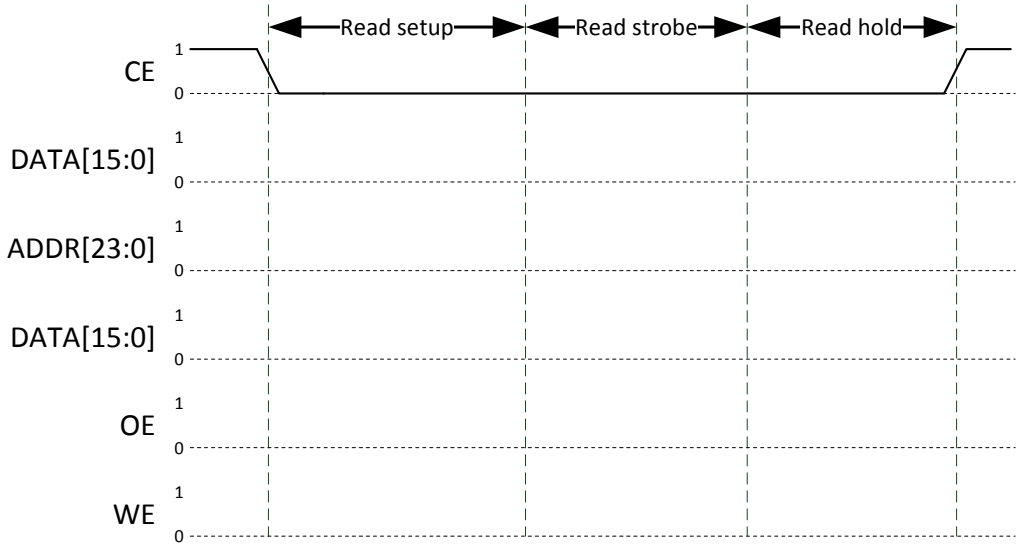
Since the bus is asynchronous, read and write accesses are taking place in three phases:

1. **Setup:** Phase between the beginning of a memory cycle (chip select low, address valid, byte enable valid, write data valid) and the activation of read or write strobe.
2. **Strobe:** Phase between the activation and deactivation of the read (OE) or write (WE) strobe.
3. **Hold:** Phase between the deactivation of the read or write strobe and the end of the cycle (which may be either an address change or the deactivation of the chip select signal.

A) Please complete the signal changes in the timing diagram below for a write access of data 0xBEEF at address 0xC00004! Consider the above named phases!



B) Please complete the signal changes in the timing diagram below for a read access at address 0xC00004! Consider the above named phases!



Task 7 Networks

Task 7.1 XY-Routing

Figure 7.1 shows a 4x4 meshed Network-on-Chip with bidirectional links for packet based communication.

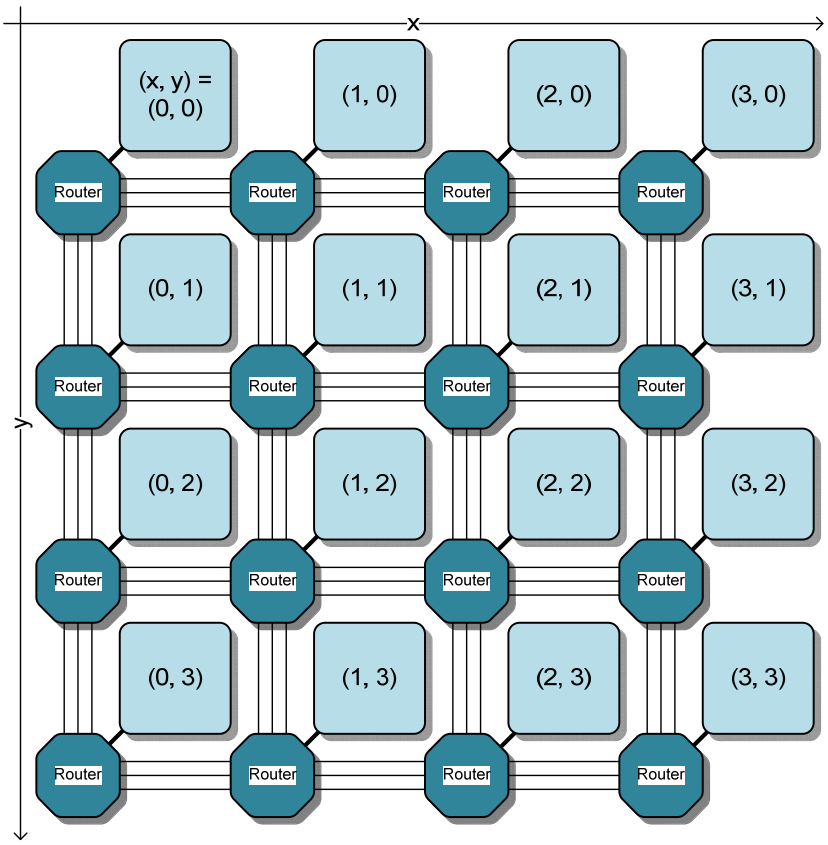


Figure 7.1: 4x4 meshed Network-on-Chip

For the following it is assumed, that XY-routing is used.

A) Which routers are passed by a packet sent from (x, y) = (1, 1) to (2, 3). Please provide the coordinates of the passed router in the order given by the transmission process.

Now, there is an error on the NoC, blocking the link between router (1, 1) and (0, 1).

B) Is router (3, 1) affected by this error? If so, which are the destination nodes to which router (3, 1) cannot communicate anymore (give the coordinates)?

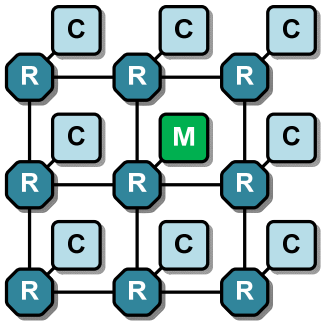
C) XY-Routing enables deadlock-freedom by avoiding turns. Which turns are these?

D) Comparing centralized and distributed routing: Give one advantage for each strategy

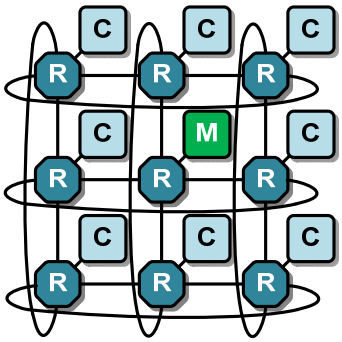
E) Besides centralized and distributed routing there exist other routing methods. Give two of them.

Task 7.2 Topologies

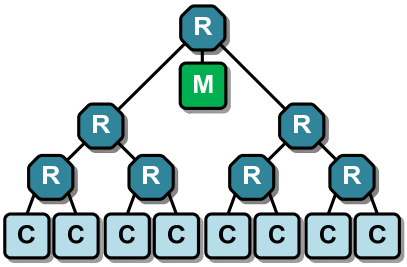
In the following three different topologies: (a) Mesh, (b) Torus and (c) Binary Tree will be investigated under different constraints. All links can be assumed to be bi-directional.



(a) Mesh



(b) Torrus



(c) Binary Tree

Select the best suitable topology and reason your choice:

A) Fair access of all nodes to a shared memory:

B) Lowest number of hops taken on average for data transmission:

C) Highest number of link error tolerable before inaccessibility of one node:

Task 7.3 Circuit- and Packet-Switching

In the following different requirements are given. Please select the switching method that fits best to the given requirement.

Requirement	Circuits-Switching	Packet-Switching
Low latency (transmission of 1 byte of data, no connections established)		
Low latency (transmission of 1 byte of data, connections established)		
Real time guarantees		
Energy Consumption		
Flexibility		
Short and non-frequent data transfers		

Task 7.4 OSI Reference Model

Figure 7.2 shows the 7 layers and the layer names of the OSI reference model

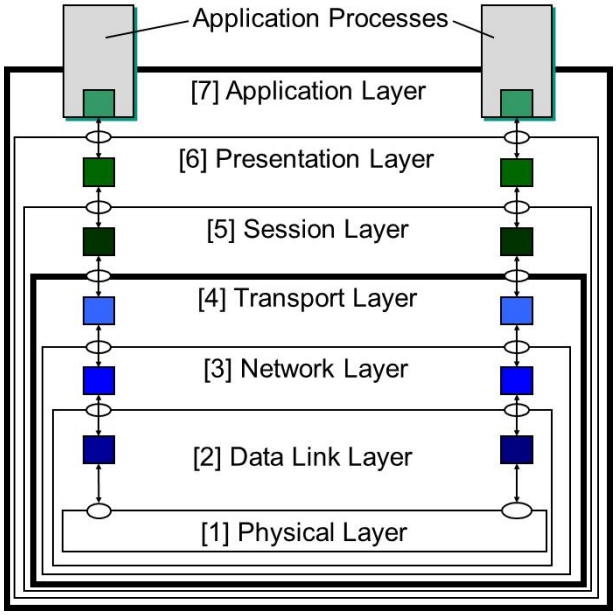


Figure 7.2: The seven layers of the OSI reference model

A) Please give the highest layer of the ISO model shown Figure 7.2, that is used by the following components:

Router:

Hub:

Repeater:

Bridge:

The following latencies for data processing within each layer of the OSI reference model can be assumed for all devices in the following:

[1] Physical Layer:	0.1 us
[2] Data Link Layer:	10 us
[3] Network Layer:	100 us
[4] Transport Layer:	0.5 ms
[5] Session Layer:	1 ms
[6] Presentation Layer:	1.5 ms
[7] Application Layer:	2.5 ms

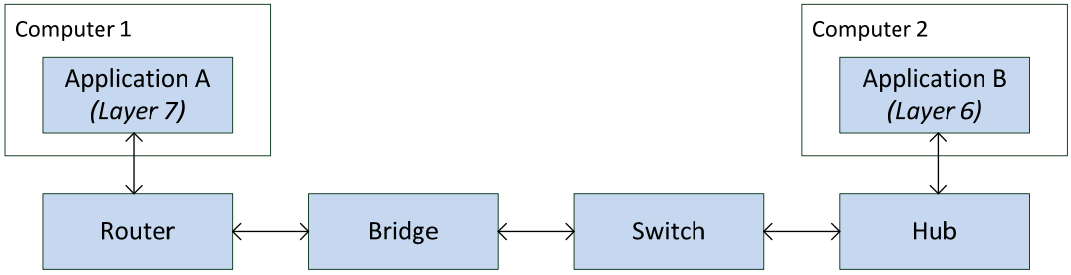


Figure 7.3: Data transmission scenario

In Figure 7.3 the communication between Application A and Application B is shown. The payload size can be assumed as small. Thus, data transmission latency is assumed to be independent from the payload size. Links between devices are short and transmission delay can be assumed to be zero. Communciation between devices is done on the physical layer.

B) Please calculate the communication latency of each device on the communication path between Application A and Application B shown in Figure 7.3.

Computer 1:

Router:

Bridge:

Switch:

Hub:

Computer 2: